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| 10/772,737 | 02/05/2004 | Claude Basso | RPS920030157US1 (IRA-10-5 | 9787 |

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| EXAMINER | |
|---|---|
| RIYAMI, ABDULLA A | |

| ART UNIT | PAPER NUMBER |
|---|---|
| 2616 | |

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**Please find below and/or attached an Office communication concerning this application or proceeding.**

The time period for reply, if any, is set in the attached communication.

Notice of the Office communication was sent electronically on above-indicated "Notification Date" to the following e-mail address(es):

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| Office Action Summary | Application No. | Applicant(s) | |
|---|---|---|---|
| | 10/772,737 | BASSO ET AL. | |
| | Examiner | Art Unit | |
| | ABDULLAH RIYAMI | 2616 | |

*-- The MAILING DATE of this communication appears on the cover sheet with the correspondence address --*

**Period for Reply**

A SHORTENED STATUTORY PERIOD FOR REPLY IS SET TO EXPIRE *3* MONTH(S) OR THIRTY (30) DAYS, WHICHEVER IS LONGER, FROM THE MAILING DATE OF THIS COMMUNICATION.

- Extensions of time may be available under the provisions of 37 CFR 1.136(a). In no event, however, may a reply be timely filed after SIX (6) MONTHS from the mailing date of this communication.
- If NO period for reply is specified above, the maximum statutory period will apply and will expire SIX (6) MONTHS from the mailing date of this communication.
- Failure to reply within the set or extended period for reply will, by statute, cause the application to become ABANDONED (35 U.S.C. § 133). Any reply received by the Office later than three months after the mailing date of this communication, even if timely filed, may reduce any earned patent term adjustment. See 37 CFR 1.704(b).

**Status**

1)☒ Responsive to communication(s) filed on *18 February 2008*.

2a)☒ This action is **FINAL**. 2b)☐ This action is non-final.

3)☐ Since this application is in condition for allowance except for formal matters, prosecution as to the merits is closed in accordance with the practice under *Ex parte Quayle*, 1935 C.D. 11, 453 O.G. 213.

**Disposition of Claims**

4)☒ Claim(s) *1-5,7-12 and 14-22* is/are pending in the application.

4a) Of the above claim(s) _____ is/are withdrawn from consideration.

5)☐ Claim(s) _____ is/are allowed.

6)☒ Claim(s) *1-5,9-12 and 14-22* is/are rejected.

7)☒ Claim(s) *7 and 8* is/are objected to.

8)☐ Claim(s) _____ are subject to restriction and/or election requirement.

**Application Papers**

9)☐ The specification is objected to by the Examiner.

10)☒ The drawing(s) filed on *18 February 2008* is/are: a)☒ accepted or b)☐ objected to by the Examiner.

Applicant may not request that any objection to the drawing(s) be held in abeyance. See 37 CFR 1.85(a).

Replacement drawing sheet(s) including the correction is required if the drawing(s) is objected to. See 37 CFR 1.121(d).

11)☐ The oath or declaration is objected to by the Examiner. Note the attached Office Action or form PTO-152.

**Priority under 35 U.S.C. § 119**

12)☐ Acknowledgment is made of a claim for foreign priority under 35 U.S.C. § 119(a)-(d) or (f).

a)☐ All b)☐ Some * c)☐ None of:

1.☐ Certified copies of the priority documents have been received.

2.☐ Certified copies of the priority documents have been received in Application No. _____.

3.☐ Copies of the certified copies of the priority documents have been received in this National Stage application from the International Bureau (PCT Rule 17.2(a)).

* See the attached detailed Office action for a list of the certified copies not received.

**Attachment(s)**

1) ☒ Notice of References Cited (PTO-892)
2) ☐ Notice of Draftsperson's Patent Drawing Review (PTO-948)
3) ☐ Information Disclosure Statement(s) (PTO/SB/08) Paper No(s)/Mail Date _____.
4) ☐ Interview Summary (PTO-413) Paper No(s)/Mail Date. _____ .
5) ☐ Notice of Informal Patent Application
6) ☐ Other: _____.

## DETAILED ACTION

This is in response to an amendment/response filed on 02/18/2008. Claims 1-3, 7, 9-12, 14-15, 17, and 22 have been amended. Claims 6, 13, and 23-24 have been cancelled. No new claims have been added. Claims 1-5, 7-12, and 14-22 remain pending in the application.

1. Applicant's arguments with respect to claims 1-5, 7-12, and 14-22 have been considered but are moot in view of the new ground(s) of rejection.

### *Claim Rejections - 35 USC § 103*

2. This application currently names joint inventors. In considering patentability of the claims under 35 U.S.C. 103(a), the examiner presumes that the subject matter of the various claims was commonly owned at the time any inventions covered therein were made absent any evidence to the contrary. Applicant is advised of the obligation under 37 CFR 1.56 to point out the inventor and invention dates of each claim that was not commonly owned at the time a later invention was made in order for the examiner to consider the applicability of 35 U.S.C. 103(c) and potential 35 U.S.C. 102(e), (f) or (g) prior art under 35 U.S.C. 103(a).

3. The factual inquiries set forth in *Graham* **v.** *John Deere Co.*, 383 U.S. 1, 148 USPQ 459 (1966), that are applied for establishing a background for determining obviousness under 35 U.S.C. 103(a) are summarized as follows:

1. Determining the scope and contents of the prior art.
2. Ascertaining the differences between the prior art and the claims at issue.
3. Resolving the level of ordinary skill in the pertinent art.
4. Considering objective evidence present in the application indicating obviousness or nonobviousness.

4. The following is a quotation of 35 U.S.C. 103(a) which forms the basis for all obviousness rejections set forth in this Office action:

> (a) A patent may not be obtained though the invention is not identically disclosed or described as set forth in section 102 of this title, if the differences between the subject matter sought to be patented and the prior art are such that the subject matter as a whole would have been obvious at the time the invention was made to a person having ordinary skill in the art to which said subject matter pertains. Patentability shall not be negatived by the manner in which the invention was made.

5. Claims 1-5 and10-12, and 14-22 are rejected under 35 U.S.C. 103(a) as being unpatentable over Lakshmanamurthy et al. (US 2004/0004964) in view of Elmaliach et al. (US 6922732) further in view of Brandt et al. (US 2002/0167957).

As per claim 1, Lakshmanamurthy et al. discloses a pipeline arrangement for a network traffic scheduler (see figure 1) comprising: a plurality of SRAM and DRAM memory devices external to the scheduler (see figure 1, blocks 142 and 144, figure 4, blocks 142-(1-n) and 144-(1-n), and paragraphs 12 and 35); Control blocks of scheduling elements stored in said memory devices with at least some of the memory devices storing more than one type of control block (see figure 1, blocks 142 and 144, figure 4, blocks 142-(1-n) and 144-(1-n), and paragraphs 12 and 35) wherein

a) SRAM memory is used if the content of a control block is Read-Modify-Write at packet enqueue and at dequeue (see paragraph 14, 17, 41, 43, 52, and 55);

b)SRAM and DRAM memory are used if the control block content is Read-Modify-Write only, at the packet dequeue (see paragraph 14,17, 41, 43, 47,51, 52, and 55); and

c)DRAM memory is used if the control block content is Read only at packet enqueue and dequeue (see paragraph 14,17, 19, 33, and 47).

Lakshmanamurthy et al. does not expressly disclose a hierarchical structure.

Elmaliach et al. discloses a hierarchical structure (see figure 1 and column 1, lines 13-50).

Lakshmanamurthy et al. and Elmaliach et al. are from the same fields of endeavor of hierarchical link sharing structures using queuing.

At the time of the invention, it would have been obvious to a person of ordinary skill in the art to use Elmaliach et al.'s hierarchical structure (see figure 1 and column 1, lines 13-50) in Lakshmanamurthy et al.'s network traffic scheduler for hierarchical link sharing using queuing.

The motivation to combine would have been to have resource allocation of the shared resource (e.g. Bandwidth) based on a set of rules that establish the share.

Lakshmanamurthy et al. and Elmaliach et al. do not expressly disclose step d) memory access allocated to enqueue tasks does not conflict with memory access allocated to dequeue tasks; Time based calendar arrays to provide guaranteed bandwidth service for flow queues; and Weighted fair queueing calendar arrays for allocation of available bandwidth for competing flows when no service is required by time base calendars.

Brandt et al. discloses memory access allocated to enqueue tasks does not conflict with memory access allocated to dequeue tasks; Time based calendar arrays to provide guaranteed bandwidth service for flow queues; and Weighted fair queueing

calendar arrays for allocation of available bandwidth for competing flows when no service is required by time base calendars (see abstract, paragraphs 93,158, and 160, weighted fair queueing process when guaranteed bandwidth is transmitted).

Brandt et al., Lakshmanamurthy et al. and Elmaliach et al. are from the same fields of endeavor of bandwidth allocation using queuing.

At the time of the invention, it would have been obvious to a person of ordinary skill in the art to use Brandt et al.'s Weighted fair queueing technique and device (see abstract, paragraphs 93,158, and 160) in Elmaliach et al.'s hierarchical structure (see figure 1 and column 1, lines 13-50) and Lakshmanamurthy et al.'s network traffic scheduler. The motivation to combine would have been to have a technique for hierarchical link sharing and bandwidth allocation using queuing, where a queue is allowed to use up to a particular upper bandwidth with that is guaranteed. The remaining bandwidth is obtained using the weighted fair queueing process. In this manner, the guaranteed bandwidth is always guaranteed and only the availability of excess bandwidth is changed.

As per claim 2, Lakshmanamurthy et al. discloses a pipeline arrangement for a network traffic scheduler (see figure 1), wherein DRAM memory is preferentially used if the Read-Modify-Write content is only at the packet dequeue (see paragraph 14, 17, 41, 43, 47, 51, 52, and 55).

As per claim 3, Lakshmanamurthy et al. discloses a pipeline arrangement for a network traffic scheduler (see figure 1), wherein the control blocks include flow queue control blocks, frame control flow blocks, hierarchy control blocks,

target port queue control blocks, and schedule control blocks (see paragraphs 11 and 12).

As per claim 4 and 5, Lakshmanamurthy et al. discloses a pipeline arrangement for a network traffic scheduler (see figure 1), a physical port bandwidth which is divided into a plurality of logical links (see paragraph 40 and figure 4), the bandwidth available to each of the logical links is divided into a plurality of VLANs (see paragraphs 40 and 26 can be implemented in VLAN). And also wherein physical port bandwidth resources for non-hierarchical links are shared among individual traffic flows (see paragraphs 12, 40 and 26).

Lakshmanamurthy et al. does not expressly disclose hierarchical link sharing and the bandwidth being shared by a plurality of individual user flows.

Elmaliach et al. discloses hierarchical link sharing and the bandwidth being shared by a plurality of individual user flows (see figure 1 and column 1, lines 13-50).

Lakshmanamurthy et al. and Elmaliach et al. are from the same fields of endeavor of hierarchical link sharing structures using queuing.

At the time of the invention, it would have been obvious to a person of ordinary skill in the art to use Elmaliach et al.'s hierarchical pipeline arrangement for link resource sharing serving multiple queues (see figure 1 and column 1, lines 13-50) in Lakshmanamurthy et al.'s network traffic scheduler for hierarchical link sharing using queuing.

The motivation to combine would have been to have resource allocation of the shared resource (e.g. Bandwidth) based on a set of rules that establish the share.

As per claim 9, Lakshmanamurthy et al. discloses a method for retrieving and pipelining information for a network traffic scheduler (see figure 1), wherein the information is stored in a plurality of SRAM and DRAM devices comprising storing functional queue control blocks in the SRAM and DRAM devices (see figure 1, blocks 142 and 144, figure 4, blocks 142-(1-n) and 144-(1-n), and paragraphs 12 and 35), wherein control block content that is Read-Modify-Write at both packet enqueue and dequeue time is stored in SRAM devices (see paragraph 14, 17, 41, 43, 52, and 55); control block content that is Read-Modify- Write packet only at dequeue time is stored in either SRAM or DRAM devices (see paragraph 14,17, 41, 43, 47,51, 52, and 55); and control block content that is read only either at enqueue or dequeue time is stored in DRAM devices (see paragraph 14,17, 19, 33, and 47).

Lakshmanamurthy et al. does not expressly disclose a hierarchical structure having two modes.

Elmaliach et al. discloses a hierarchical structure having two modes (see figure 1 and column 1, lines 13-50).

Lakshmanamurthy et al. and Elmaliach et al. are from the same fields of endeavor of hierarchical link sharing structures using queuing.

At the time of the invention, it would have been obvious to a person of ordinary skill in the art to use Elmaliach et al.'s hierarchical structure (see figure 1 and column 1, lines 13-50) in Lakshmanamurthy et al.'s network traffic scheduler for hierarchical link sharing using queuing.

The motivation to combine would have been to have resource allocation of the shared resource (e.g. Bandwidth) based on a set of rules that establish the share.

Lakshmanamurthy et al. and Elmaliach et al. do not expressly disclose step d) memory access allocated to enqueue tasks does not conflict with memory access allocated to dequeue tasks; Time based calendar arrays to provide guaranteed bandwidth service for flow queues; and Weighted fair queueing calendar arrays for allocation of available bandwidth for competing flows when no service is required by time base calendars.

Brandt et al. discloses memory access allocated to enqueue tasks does not conflict with memory access allocated to dequeue tasks; Time based calendar arrays to provide guaranteed bandwidth service for flow queues; and Weighted fair queueing calendar arrays for allocation of available bandwidth for competing flows when no service is required by time base calendars (see abstract, paragraphs 93,158, and 160, weighted fair queueing process when guaranteed bandwidth is transmitted).

Brandt et al., Lakshmanamurthy et al. and Elmaliach et al. are from the same fields of endeavor of bandwidth allocation using queuing.

At the time of the invention, it would have been obvious to a person of ordinary skill in the art to use Brandt et al.'s Weighted fair queueing technique and device (see abstract, paragraphs 93,158, and 160) in Elmaliach et al.'s hierarchical structure (see figure 1 and column 1, lines 13-50) and Lakshmanamurthy et al.'s network traffic scheduler. The motivation to combine would have been to have a technique for hierarchical link sharing and bandwidth allocation using queuing, where a queue is

allowed to use up to a particular upper bandwidth with that is guaranteed. The remaining bandwidth is obtained using the weighted fair queueing process. In this manner, the guaranteed bandwidth is always guaranteed and only the availability of excess bandwidth is changed.

As per claim 10 and 11, Lakshmanamurthy et al. discloses a method for retrieving and pipelining information for a network traffic scheduler (see figure 1), a physical port bandwidth which is divided into a plurality of logical links (see paragraph 40 and figure 4), the bandwidth available to each of the logical links is divided into a plurality of VLANs (see paragraphs 40 and 26 can be implemented in VLAN). And also wherein physical port bandwidth resources for non-hierarchical links are shared among individual traffic flows (see paragraphs 40 and 26).

Lakshmanamurthy et al. does not expressly disclose hierarchical link sharing and the bandwidth being shared by a plurality of individual user flows.

Elmaliach et al. discloses hierarchical link sharing and the bandwidth being shared by a plurality of individual user flows (see figure 1 and column 1, lines 13-50).

Lakshmanamurthy et al. and Elmaliach et al. are from the same fields of endeavor of hierarchical link sharing structures using queuing.

At the time of the invention, it would have been obvious to a person of ordinary skill in the art to use Elmaliach et al.'s hierarchical pipeline arrangement for link resource sharing serving multiple queues (see figure 1 and column 1, lines 13-50) in Lakshmanamurthy et al.'s network traffic scheduler for hierarchical link sharing using queuing.

The motivation to combine would have been to have resource allocation of the shared resource (e.g. Bandwidth) based on a set of rules that establish the share.

As per claim 12, Lakshmanamurthy et al. discloses a structure for a hardware scheduler pipeline (see figure 1) comprising a plurality of control blocks (see figure 1, blocks 142 and 144, figure 4, blocks 142-(1-n) and 144-(1-n), and paragraphs 12 and 35); a plurality of memory devices external to the scheduler in which the control blocks are stored, the memory devices comprise both SRAM and DRAM (see figure 1, blocks 142 and 144, figure 4, blocks 142-(1-n) and 144-(1-n), and paragraphs 12 and 35), at least some of the memory devices sharing more than one type of control block (see paragraph 12).

Lakshmanamurthy et al. does not expressly disclose a hierarchical pipeline arrangement for link resource sharing serving multiple queues.

Elmaliach et al. discloses a hierarchical pipeline arrangement for link resource sharing serving multiple queues (see figure 1 and column 1, lines 13-50).

Lakshmanamurthy et al. and Elmaliach et al. are from the same fields of endeavor of hierarchical link sharing structures using queuing.

At the time of the invention, it would have been obvious to a person of ordinary skill in the art to use Elmaliach et al.'s hierarchical pipeline arrangement for link resource sharing serving multiple queues (see figure 1 and column 1, lines 13-50) in Lakshmanamurthy et al.'s network traffic scheduler for hierarchical link sharing using queuing.

The motivation to combine would have been to have resource allocation of the shared resource (e.g. Bandwidth) based on a set of rules that establish the share.

Lakshmanamurthy et al. and Elmaliach et al. do not expressly disclose using time based calendar arrays and weighted fair queueing calendar arrays for allocation of available bandwidth between said memory devices.

Brandt et al. discloses using time based calendar arrays and weighted fair queueing calendar arrays for allocation of available bandwidth between said memory devices (see abstract, paragraphs 93,158, and 160, weighted fair queueing process when guaranteed bandwidth is transmitted).

Brandt et al., Lakshmanamurthy et al. and Elmaliach et al. are from the same fields of endeavor of bandwidth allocation using queuing.

At the time of the invention, it would have been obvious to a person of ordinary skill in the art to use Brandt et al.'s Weighted fair queueing technique and device (see abstract, paragraphs 93,158, and 160) in Elmaliach et al.'s hierarchical structure (see figure 1 and column 1, lines 13-50) and Lakshmanamurthy et al.'s network traffic scheduler. The motivation to combine would have been to have a technique for hierarchical link sharing and bandwidth allocation using queuing, where a queue is allowed to use up to a particular upper bandwidth with that is guaranteed. The remaining bandwidth is obtained using the weighted fair queueing process. In this manner, the guaranteed bandwidth is always guaranteed and only the availability of excess bandwidth is changed.

As per claim 14, the control blocks include, flow queue control blocks, frame control blocks, calendar control blocks, target port queue control blocks, and hierarchy control blocks (see paragraphs 11 and 12).

As per claim 15, the control blocks that are accessed less frequently within a fixed period of time are stored in DRAM memories, and control blocks that are accessed with higher frequency within a fixed period of time are stored in SRAM (see paragraph 12).

As per claim 16, basic flow QCB is stored in SRAM memory (see paragraph 14, 17, 41, 43, 52, and 55) and dequeue/enqueue read only flow QCB is stored in DRAM memory (see paragraph 14, 17, 19, 33, and 47).

As per claim 17, Lakshmanamurthy et al. discloses a method for retrieving and pipelining information for a network traffic scheduler (see figure 1), a physical port bandwidth which is divided into a plurality of logical links (see paragraph 40 and figure 4), the bandwidth available to each of the logical links is divided into a plurality of VLANs (see paragraphs 40 and 26 can be implemented in VLAN).

Lakshmanamurthy et al. does not expressly disclose hierarchical link sharing and the bandwidth being shared by a plurality of individual user flows.

Elmaliach et al. discloses hierarchical link sharing and the bandwidth being shared by a plurality of individual user flows (see figure 1 and column 1, lines 13-50).

Lakshmanamurthy et al. and Elmaliach et al. are from the same fields of endeavor of hierarchical link sharing structures using queuing.

At the time of the invention, it would have been obvious to a person of ordinary skill in the art to use Elmaliach et al.'s hierarchical pipeline arrangement for link resource sharing serving multiple queues (see figure 1 and column 1, lines 13-50) in Lakshmanamurthy et al.'s network traffic scheduler for hierarchical link sharing using queuing.

The motivation to combine would have been to have resource allocation of the shared resource (e.g. Bandwidth) based on a set of rules that establish the share.

As per claim 18, time-based calendar arrays for guaranteed bandwidth service and weighted fair queueing calendar arrays for allocation of available bandwidth for competing flows at each port when no service is required by the time-based calendars (see figure 1, well known that scheduler program may use weighted round robin scheduling algorithm or any other type of scheduling algorithm).

As per claim 19, each of the calendar arrays contains three pointers comprising a current position pointer, a current time pointer and a next position pointer each of the calendar arrays (see paragraph 55).

As per claim 20, the time-based calendar provides a scheduling function for flow queues and VLANs (see paragraphs 40 and 26 can be implemented in VLAN).

As per claim 21, the weighted fair queueing calendar provides best effort scheduling in flow queues, VLANs and logical links (see figure 1, well known that scheduler program may use weighted round robin scheduling algorithm or any other type of scheduling algorithm).

Claims 22 is rejected under 35 U.S.C. 103(a) as being unpatentable over Lakshmanamurthy et al. (US 2004/0004964) in view of Brandt et al. (US 2002/0167957).

As per claim 22, Lakshmanamurthy et al. discloses an article of manufacture comprising a computer usable medium having a computer readable program embodied in the medium, wherein the computer readable program, when executed on a computer (see paragraph 60), causes the scheduler to store functional queue control blocks in external memory storage devices comprising a mix of SRAM and DRAM devices based on the block content at enqueue and dequeue time (see paragraphs 11-15 and 55), and to share the external devices among the control blocks (see figure 1, blocks 142 and 144, figure 4, blocks 142-(1-n) and 144-(1-n), and paragraphs 12 and 35), said computer readable program further causes a control block content having Read-Modify-Write at both enqueue and dequeue time to be stored in SRAM (see paragraph 14,17, 41, 43, 47,51, 52, and 55); a control block content having Read- Modify-Write at only dequeue time to be stored in either SRAM or DRAM (see paragraph 14,17, 41, 43, 47,51, 52, and 55); and a control block content having 'read' only to be stored in DRAM (see paragraph 14,17, 41, 43, 47,51, 52, and 55), and said program causes the scheduler to select a flow queue to egress for each duration of a scheduler tick using a time-based calendar or a weighted fair queueing calendar.

Lakshmanamurthy et al. et al. does not expressly disclose a program causing the scheduler to select a flow queue using time based calendar arrays and weighted fair

queueing calendar arrays for allocation of available bandwidth between said memory devices.

Brandt et al. discloses a program causing the scheduler to select a flow queue using time based calendar arrays and weighted fair queueing calendar arrays for allocation of available bandwidth between said memory devices (see abstract, paragraphs 93,158, and 160, weighted fair queueing process when guaranteed bandwidth is transmitted).

Brandt et al. and Lakshmanamurthy et al. et al. are from the same fields of endeavor of bandwidth allocation using queuing.

At the time of the invention, it would have been obvious to a person of ordinary skill in the art to use Brandt et al.'s Weighted fair queueing technique and device (see abstract, paragraphs 93,158, and 160) in Lakshmanamurthy et al.'s network traffic scheduler. The motivation to combine would have been to have a technique for bandwidth allocation using queuing, where a queue is allowed to use up to a particular upper bandwidth with that is guaranteed. The remaining bandwidth is obtained using the weighted fair queueing process. In this manner, the guaranteed bandwidth is always guaranteed and only the availability of excess bandwidth is changed.

***Allowable Subject Matter***

6. Claims 7 and 8 are objected to as being dependent upon a rejected base claim, but would be allowable if rewritten in independent form including all of the limitations of the base claim and any intervening claims.

***Conclusion***

7. The prior art made of record and not relied upon is considered pertinent to applicant's disclosure. See form 892.

8. Applicant's amendment necessitated the new ground(s) of rejection presented in this Office action. Accordingly, **THIS ACTION IS MADE FINAL**. See MPEP § 706.07(a). Applicant is reminded of the extension of time policy as set forth in 37 CFR 1.136(a).

A shortened statutory period for reply to this final action is set to expire THREE MONTHS from the mailing date of this action. In the event a first reply is filed within TWO MONTHS of the mailing date of this final action and the advisory action is not mailed until after the end of the THREE-MONTH shortened statutory period, then the shortened statutory period will expire on the date the advisory action is mailed, and any extension fee pursuant to 37 CFR 1.136(a) will be calculated from the mailing date of the advisory action. In no event, however, will the statutory period for reply expire later than SIX MONTHS from the date of this final action.

Any inquiry concerning this communication or earlier communications from the examiner should be directed to ABDULLAH RIYAMI whose telephone number is (571)270-3119. The examiner can normally be reached on Monday through Thursday 8am-5pm EST.

If attempts to reach the examiner by telephone are unsuccessful, the examiner's supervisor, Huy D. Vu can be reached on (571) 272-3155. The fax phone number for the organization where this application or proceeding is assigned is 571-273-8300.

Information regarding the status of an application may be obtained from the Patent Application Information Retrieval (PAIR) system. Status information for published applications may be obtained from either Private PAIR or Public PAIR. Status information for unpublished applications is available through Private PAIR only. For more information about the PAIR system, see http://pair-direct.uspto.gov. Should you have questions on access to the Private PAIR system, contact the Electronic Business Center (EBC) at 866-217-9197 (toll-free). If you would like assistance from a USPTO Customer Service Representative or access to the automated information system, call 800-786-9199 (IN USA OR CANADA) or 571-272-1000.

/Abdullah Riyami/
Examiner, Art Unit 2616

/Huy D. Vu/

Supervisory Patent Examiner, Art Unit 2616